15.   (Amended) The article of claim 13 further storing instructions that, if executed, enable a processor-based system to monitor an input queue and fetch one type of packet to bypass another type of packet for transmission.

17.   (Amended) The article of claim 13 further storing instructions that, if executed, enable a processor-based system to receive packets to be transmitted in a first in first out memory, check each packet to determine its security status and provide a pointer to the packet based on its security status.

18.   (Amended) The article of claim 17 further storing instructions that, if executed, enable a processor-based system to organize a plurality of packets in a first in first out memory as a linked list of packet blocks.

19.   (Amended) The article of claim 18 further storing instructions that, if executed, enable a processor-based system to mark each of said packet blocks in said first in first out memory as being either a security packet or a non-security packet.

20.   (Amended) The article of claim 19 further storing instructions that, if executed, enable a processor-based system to mark packets as security or non-security packets depending on the attributes that are indicated in an internet protocol header associated with each packet.

21.   (Amended) The article of claim 20 further storing instructions that, if executed, enable a processor-based system to provide a pointer that points to a security packet.

22.   (Amended) The article of claim 21 further storing instructions that, if executed, enable a processor-based system to provide pointers for non-security packets and to select between pointers to security packets and non-security packets for transmission of said packets.

23.   (Amended) The article of claim 22 further storing instructions that, if executed, enable a processor-based system to select among pointers based on a round robin priority basis.